What is claimed is:

1. A cache memory, comprising:

a data storage capable of storing data which requires consistency of data with a main memory; and

a storage controller which controls to store data which does not require consistency of data with said main memory in an arbitrary data region in said data storage.

2. The cache memory according to claim 1, wherein said arbitrary data region is a data region designated by a programmer.

3. The cache memory according to claim 1, further comprising:

a region designating unit which specifies addresses of said data region for storing data which does not require consistency of data with said main memory; and

an address coincidence determination unit which determines whether or not the designated address coincides with the addresses designated by said region designated unit.

4. The cache memory according to claim 3, further comprising a tag unit which stores addresses of data stored in said data storage,

wherein said data storage and said tag unit are composed of a plurality of ways including a plurality of indexes, respectively; and

said region designated unit specifies whether or not data which does not require consistency of data with said main memory is stored in the corresponding data region unit is a unit of one way.

5. The cache memory according to claim 4, further comprising:

a refill information storage which stores history information of refill in said data storage; and

a refill object selector which selects ways to be refilled based on the history information stored in said refill information storage and addresses designated by said region designating unit.

6. The cache memory according to claim 5, wherein region designated unit includes:

an address setting unit provided for each way, which sets addresses of data region for storing data which does not require consistency of data with said main memory; and

a setting information storage provided for each way, which stores flag information indicative of whether or not a prescribed address is set to said address setting unit,

wherein said refill object selector selects the way to be refilled based on the refill history information and the flag information.

7. The cache memory according to claim 1, wherein a look-aside type connection method in which said main memory and said cache memory are connected to a common system bus, and a write-through writing method in which data is written to said main memory and said cache memory at the same time are adopted.

8. A processor which adopts a look-aside type connection method in which a main memory and a cache memory are connected to a common system bus, and a write-through writing method in which data is written to said main memory and said cache memory at the same time, wherein said cache memory includes:

a data storage capable of storing data which requires consistency of data with said main memory; and

a storage controller which controls to store data which does not require consistency of data with said main memory, in an arbitrary data region in said data storage.

9. The processor according to claim 8, wherein said arbitrary data region is a data region designated by a programmer.

10. The processor according to claim 8, further comprising:

a region designated unit which specifies addresses of said data region to store data which does not require consistency of data with said main memory; and

an address coincidence determination unit which determines whether or not the designated address coincides with the address designated by said region designated unit.

11. The processor according to claim 10, further comprising a tag unit which stores addresses of data stored in said data storage,

wherein said data storage and said tag unit are composed of a plurality of ways including a plurality of indexes, respectively; and

said region designated unit specifies whether or not data which does not require consistency of data with said main memory is stored in the corresponding data region unit is a unit of one way.

12. The processor according to claim 11, further comprising:

a refill information storage which stores history information of refill in said data storage; and

a refill object selector which selects ways to be refilled based on the history information stored in said refill information storage and addresses designated by said region designating unit.

13. The processor according to claim 12, wherein region designated unit includes:

an address setting unit provided for each way, which

sets addresses of data region for storing data which does not require consistency of data with said main memory; and

a setting information storage provided for each way, which stores flag information indicative of whether or not a prescribed address is set to said address setting unit,

wherein said refill object selector selects the way to be refilled based on the refill history information and the flag information.

14. A cache control method which adopts a look-aside type connection method in which a main memory and a cache memory are connected to a common system bus, and a write-through writing method in which data is written into said main memory and said cache memory at the same time, comprising controlling to store data which does not require consistency of data with said main memory in an arbitrary data region in a data storage to store data which does not require consistency of data said main memory.

15. The cache control method according to claim 14, wherein said arbitrary data region is a data region designated by a programmer.

16. The cache control method according to claim 14, further comprising:

designating in advance addresses of said data region to store data which does not require consistency of data with said main memory; and

determining whether or not required address coincides with the designated address.

17. The cache control method according to claim 16, wherein said data storage and a tag unit which stores addresses of data stored in said data storage are composed of a plurality of ways including a plurality of indexes; and

it is designated whether or not data which does not

require consistency of data with said main memory is stored in the corresponding data region unit in unit of one way.

18. The cache control method according to claim 17, further comprising:

storing history information of refill in said data storage; and

selecting the way to be refilled based on the stored history information and the address designated by said region designated unit.

19. The cache control method according to claim 18, comprising:

setting addresses of a data region to store data which does not require consistency of data with said main memory for each way;

storing the flag information indicative of whether or not addresses are set for each way; and

selecting the way to be refilled based on said refill history information and said flag information.